241190US2

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: : ATTN:

Takeshi YOSHIDA : EXAMINER: DILLARD, Delora

SERIAL NO.: 10/632,866 : GROUP ART UNIT: N/A

FILED: August 4, 2003

TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING SYSTEM BUS DIVIDED IN STAGES

ATTORNEY DECLARATION

COMMISSIONER FOR PATENTS
Alexandria, VA 22313-1450

Robert T. Pous
Registration No. 29,099

Sir:

I, ~~Marvin J. Spivak~~, attorney of record in the above-identified application, declare the attached to be a true and accurate copy of the Application as filed on August 4, 2003.

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: 2/23/04

Marvin J. Spivak
Registration No. 24,913
Attorney of Record

Customer Number
22850
(703) 413-3000
MJS/dgh
I:\USER\DGHOD\HAND CARRY TO EX\241190US ATTY DEC.DOC

Robert T. Pous
Registration No. 29,099